Hybrid CMOS System-on-Chip / InP MMIC Systems for Deep-Space Planetary Exploration at mm-Wave and THz

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Abstract — this paper discusses the applicability of hybrid CMOS/InP-MMIC mm-Wave systems to remote sensing instrumentation for space exploration in Earth and Planetary science. We review the need for lower power and lighter weight instruments to accommodate the limited payload resources of exploration spacecraft, and then demonstrate how hybrid systems can address these challenges. An example hybrid CMOS-InP radiometer operating at 100 GHz is discoursed in detail including circuit & system design, interfacing and packaging techniques. Measurements are presented showing that the hybrid approach does not compromise instrument sensitivity.

Index Terms — Radiometer, Hybrid, mm-wave, CMOS SoC

I. CHALLENGES OF CURRENT SPACECRAFT INSTRUMENTS

While many places in the solar system have yet to be explored, several moons in the outer solar system have become increasingly interesting as an exploration target for NASA. In particular, Jupiter and its moon Europa, and Saturn and its moon Enceladus are of interested as they both show evidence of stable sub-surface liquids. These sub-surface "oceans" offer temperatures and salinity conditions that may serve as an abode for extra-terrestrial life, making them a priority for future exploration missions [1].

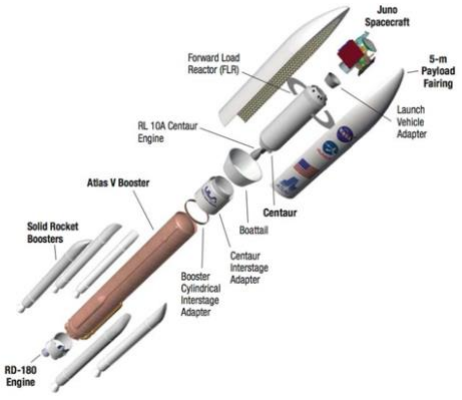

Fig 1. Atlas 551 V heavy launch vehicle used for NASA's Juno mission to study Jupiter.

In order to explore these outer planetary systems, NASA sends both flyby and orbiting spacecraft (and may eventually send landers or rovers) which have extremely limited payload resources in terms of size, weight and power. Size and weight of a spacecraft system is extremely limited because they must be accommodated by the launch vehicle which transports the spacecraft to space from the surface of the Earth. Fig 1. Shows the Atlas 551 heavy launch vehicle, which was used for Juno, NASA's most recent planetary mission to Jupiter. While the entire Atlas launch vehicle is large (58m tall), the actual spacecraft portion is a tiny fraction of this (<10% by weight) and (<5% by volume). All of the spacecraft systems including power generation and management, communication systems, and especially science instrumentation must accommodate these volume and weight restrictions.

Fig 2. Approximate size of the sun (and relative available solar energy) at various locations in our solar system and relative angular size in arc-minutes.

A second major challenge in designing communication and instrument systems for planetary missions is the limited power resources available on-board the spacecraft. Figure 2 shows the relative size of our Sun in the sky from various positions in the universe. As seen in the figure, when you move from Earth's position outward into the solar system (and away from the sun), the solar power collected by solar-cell arrays becomes quite limited, placing restrictions on the overall power consumption of spacecraft communication and instruments. Use of an Radioisotope Thermal Generator (RTG) like those on the Voyager Spacecraft or Mars Science Laboratory's Curiosity rover, can provide several 100 watts at most (ultimately again limited by volume/weight), still greatly restricting the number of systems and instrument that can be carried and operated simultaneously during critical moments of the mission.

II. CMOS FOR RADIOMETER INSTRUMENTS

Radiometers are an important remote sensing instrument for space exploration, especially those operated at mm-wave frequencies. These mm-wave instruments allow for remote measurements of a planet's atmospheric pressure from an orbiting spacecraft, as well as the detection of key gasses and even wind measurements through evaluating Doppler shifts.

The millimeter-wave frequency regime in particular contains many spectral responses for organics and other key molecules, making it an ideal place for radiometric observation. Currently InP technology based mm-wave radiometers can achieve noise temperatures as low as 350ºK. An example of a state of art radiometer is the HAMSR instrument [2] from JPL (shown in Fig. 3) where InP LNAs are used as preamplifiers along with InP MMIC downconverters. Also, a dielectric-resonance based oscillator (DRO) is used to provide the LO. While this existing instrument provides high radiometric sensitivity, the receiver is over 2.5 Kg of mass and consumes over 10W of DC power stressing payload resources.

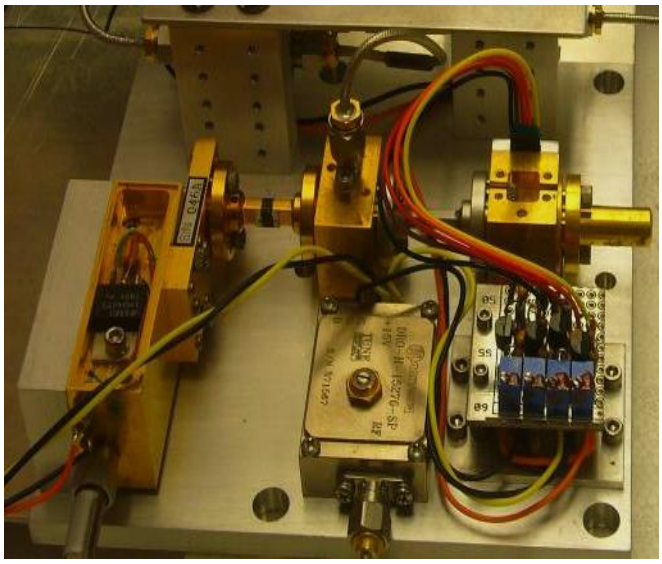

Fig 3. An existing JPL InP based radiometer from **[2]** achieving 350^{o}K noise temperature when measured at room temperature.

CMOS has made tremendous gains in mm-wave capabilities due to aggressive technology scaling during recent years with full transceivers demonstrated well beyond 50 GHz [3,4,5]**.** These advanced CMOS mm-wave technologies and more specifically the system-on-chip (SoC) capabilities which CMOS brings to the mm-wave arena can potentially address these payload size and weight challenges created by the discrete components currently used for implementing mm-wave and THz radiometers. However despite their low power and size advantages, the noise temperatures of CMOS-based receivers (on the order of 3000Kº in the latest 28nm technologies **[6]**) are not compatible with radiometric observations as the resulting brightness contrast at these high noise temperatures would be prohibitive to the typical (0.1K to 1K) temperature resolution (NEΔT) demanded by most remote sensing observations. As a solution JPL has developed a hybrid approach (first proposed in [7]) for compact radiometers where a front-end InP LNA stage is used as a pre-amplifier for a CMOS receiver allowing an instrument to maintain noise temperatures in the ranges InP technology can provide, while still taking advantage of the size and weight savings of CMOS SoC technology. A block diagram of the developed 100 GHz radiometer instrument is shown in Fig 4.

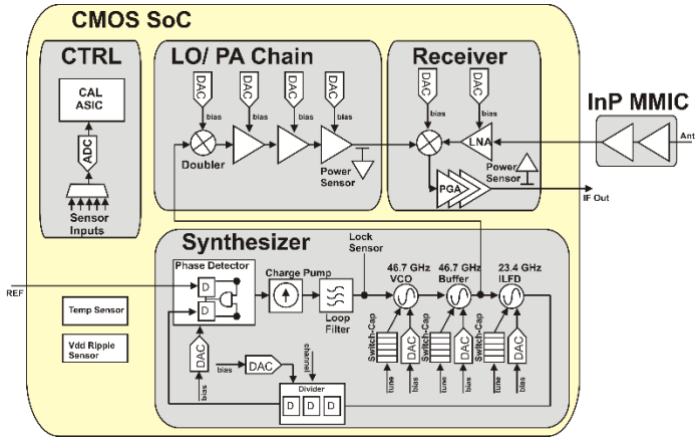

Fig 4. Block diagram of the hybrid radiometer showing CMOS SoC and external InP MMIC preamplifier.

As shown in Fig. 4 our overall radiometer system based on a heterodyne receiver architecture which offers improved sensitivity over their direct-detection counterparts [2]. First, a 40-50 GHz on-chip frequency synthesizer that is locked to an externally provided 50 MHz reference which drives a W-band push-push frequency doubler. The doubler circuit drives an transformer (XMFR)-coupled PA, and down-conversion mixer. At the IF port of the mixer, a multi-stage programmable gain amplifier is implemented to provide IF signal amplification. Several power, temperature, and lock detection sensors are placed throughout the CMOS SoC to monitor key signals, while frequency and bias tuning conditions of each amplifier and LO stage, are established by a collection of R2R DACs. The SoC includes a 10 bit low speed ADC to digitize each sensor output as well as a small calibration digital-core which runs several algorithms to calibrate for the effects of process and temperature variation.

Also critical to implementing a sensitive and low-noise heterodyne radiometer, is providing a stable LO that is free from any type of envelope modulation. To achieve this, we place a power sensor on the output of the LO circuitry which is monitored in close-loop fashion by the ADC and calibration digital circuitry during normal operation. Actuation for this control loop is provided by DACs which control biasing conditions on the 100 GHz pre-amplifier which appears before the mixer's LO port. Bandwidth of this control loop is 5 MHz. The LO power amplifier is implemented as a 3 stage XMFR-based "Caterpillar" amplifier where biasing is provided by R2R DACs connected to the transformer center-taps. This configuration allows maximum DC stability (as the transformer windings are uncoupled at DC) and also allows the DC conditions to be applied without a tuned network as there is no RF signal (propagates in odd mode) at the center tap points, as outlined in Fig 5.

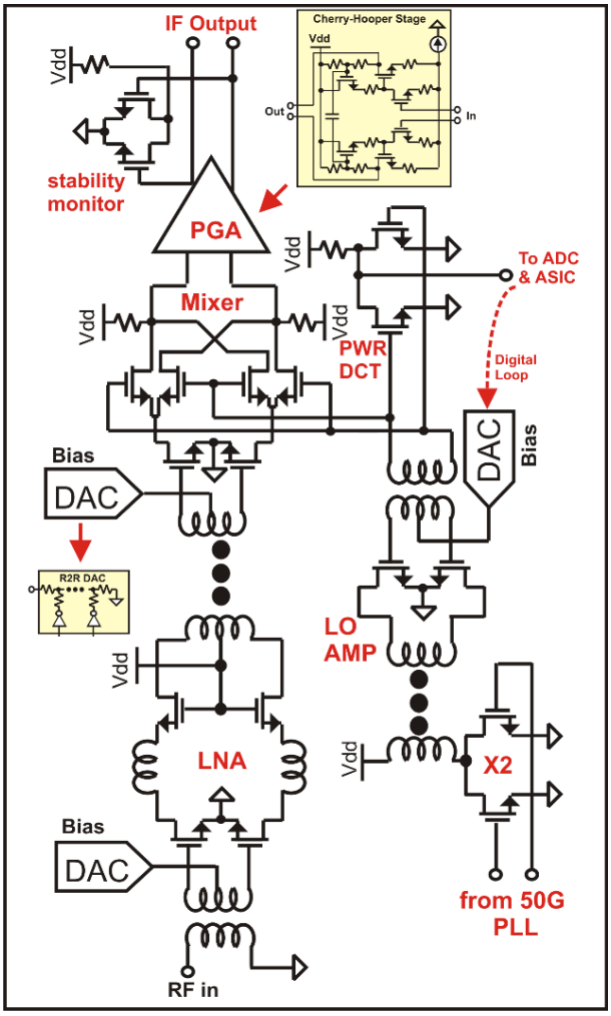

Fig 5. Detailed mm-wave schematic of the CMOS SoC receiver chain showing key sensors, detectors, control loops, and R2R control DACs.

The CMOS chip has an input LNA chain (which follows the InP preamp) and is implemented as a cascode version of the XMFR coupled amplifier. During the chip initialization, the power sensor at the IF port monitors the receiver output for any large signal tones to detect potential instability (oscillations) in the LNA/IF amp, and then adjusts the bias conditions to eliminate them. This approach allows the source and load stable condition of the mm-wave amplifiers to be conditionally satisfied during operation without sacrificing the performance losses associated with over-stabilized designs. While the CMOS LNA can achieve over 30 dB of gain when bias and tuning conditions are optimized, gain compression conditions develop when the LNA coupled to the equally high gain InP MMIC preamplifiers. To overcome this, the CMOS LNA is intentionally biased so that it is limited to 6 dB gain in total, alleviating the compression condition.

Interfacing – One of the most challenging aspects of the hybrid system is the packaging and interfacing of the CMOS SoC's to the InP MMIC based pre-amp. To accomplish this we use a standard WR10 waveguide package for the MMIC, while the CMOS is placed in a custom package that adapts its coplanar (GSG) output port to a WR10 flange (Fig. 6 & 7). The package is a metal block similar to MMIC packaging, except that it contains an entire PCB with all the support circuitry (regulators, USB interface, clock, control, …) and the CMOS chip epoxied on the PCB surface. The low speed and control interfaces of the chip are wire-bonded directly to the PCB. The metal block enclosing the PCB carries a WR10 channel and flange which aligns with the CMOS chip. Coupling between the input WR10 waveguide channel and the GSG input on the SoC is accomplished by a small probe and micro-strip line fabricated on an alumina substrate. While not independently measured, this probe coupler exhibits a loss of 3-4 dB in simulation, which is not critical as the preceding MMIC LNAs offer well over 25 dB of gain, negating these losses and their impacts on receiver noise. Once assembled the packaged CMOS SoC is directly coupled to the InP preamps with standard WR-10 waveguide. The WR10 input horn is also shown which ultimately feeds a larger reflector.

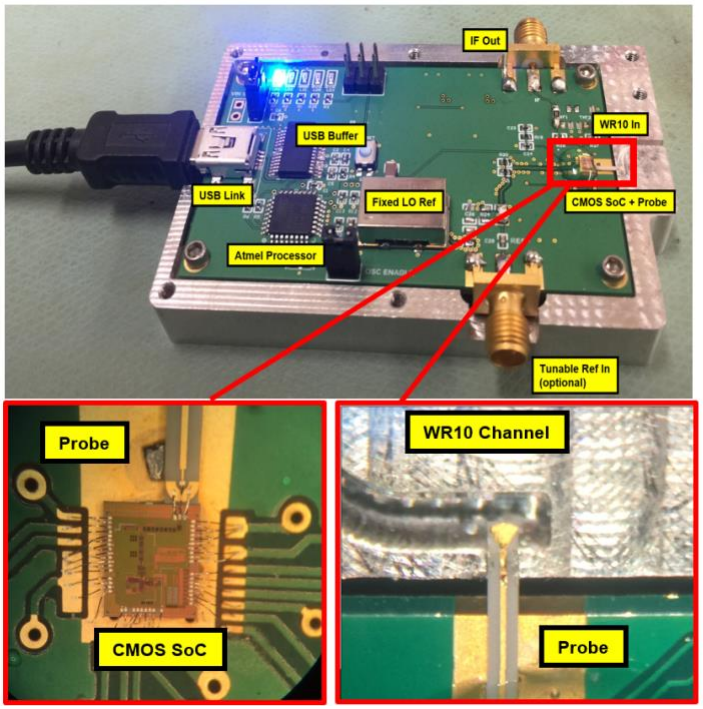

Fig 6. Custom mm-wave packaging of the CMOS SoC radiometer to provide interfacing to a standard WR-10 waveguide package.

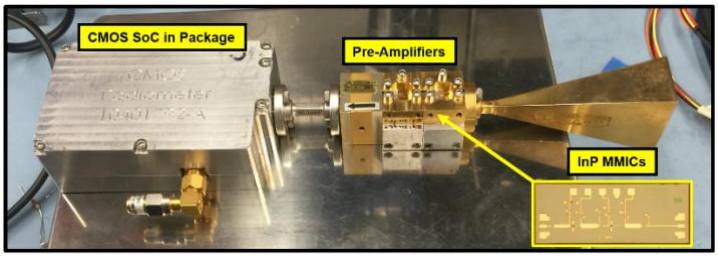

Fig 7. Full radiometer instrument with packaged CMOS SoC (from Fig 6) and InP pre-amplifier LNAs interfaced together with WR10 waveguide.

III. Sensitivity of CMOS-InP hybrid radiometer

In order to evaluate the hybrid radiometer's sensitivity we performed several receiver measurements with and without the InP preamp included in the setup. Measurements of noise figure were completed with a WR10 noise source (Quinstar QNS10 series) directly mated with the InP WR-10 input (antenna is removed in these tests). An excess noise ratio of 22 dB was applied and the Y-factor method was employed to estimate receiver noise in each case. Results of both measurements are shown in Figure 8, where for each condition, the receiver LO was swept across the entire locking range of the on-chip frequency synthesizer (the LO is unlocked outside the measured range). Measurements demonstrate that the overall noise figure is comparable to what is achievable with a fully InP based system, an expected result as the first stage (InP in both cases) dominates Rx noise.

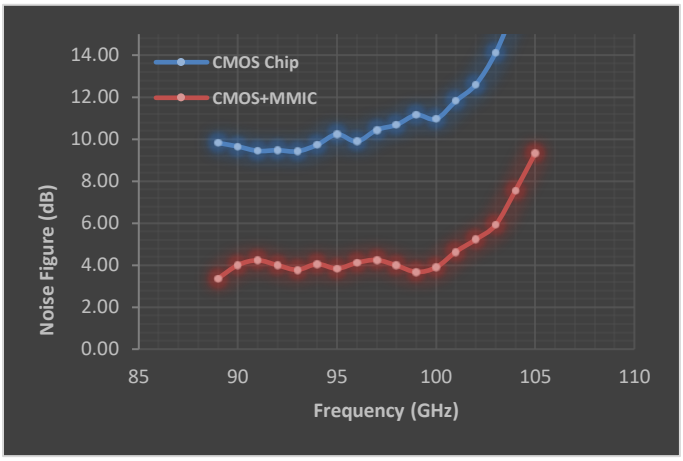

Fig 8. Measured noise figure of the CMOS SoC radiometer with and without the InP MMIC pre-amplifiers present.

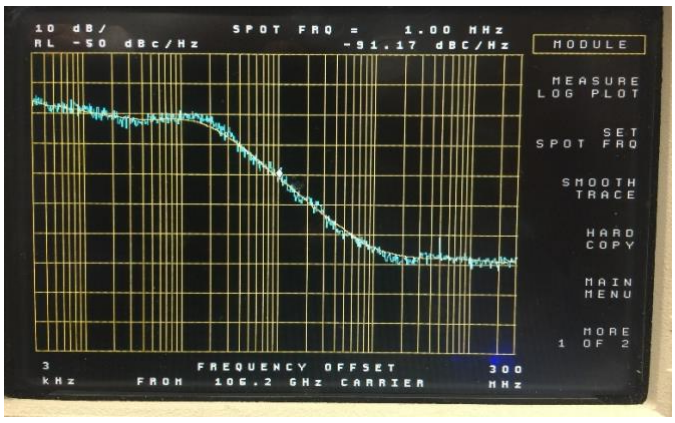

Fig 9. Measured phase noise of the CMOS synthesizer and LO integrated within the SoC radiometer chip.

A second version of the CMOS SoC was also fabricated with the receiver chain (mixer/LNA/IF) removed which simply outputs the LO signal directly to a WR-10 port. This chip was packaged in a similar fashion and can be used as a stand-alone synthesizer for other instruments built out of discrete components. This second chip allows us to directly measure the phase noise of the radiometer chip's internal synthesizer/LO chain as shown in Fig 9.

IV. Summary

In this article we have discussed the size weight and power limitations for space instruments and identified how CMOS SoCs can help address these problems provided science fidelity is not affected. We have demonstrated that using hybrid InP/CMOS systems allows the noise performance of a full InP system to be maintained while providing power reduction through the use of a CMOS receiver chain, downconverter, IF chain, and synthesizer. The demonstrated hybrid radiometer achieves a noise temperature of 352ºK comparable to a state-art-InP system (350ºK), consumes only 257mW and weighs only 0.3 Kg. As a reference the state-of-art JPL InP system in [2] consumes >10W and weighs 2.5Kg.

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